



Integrated Device Technology

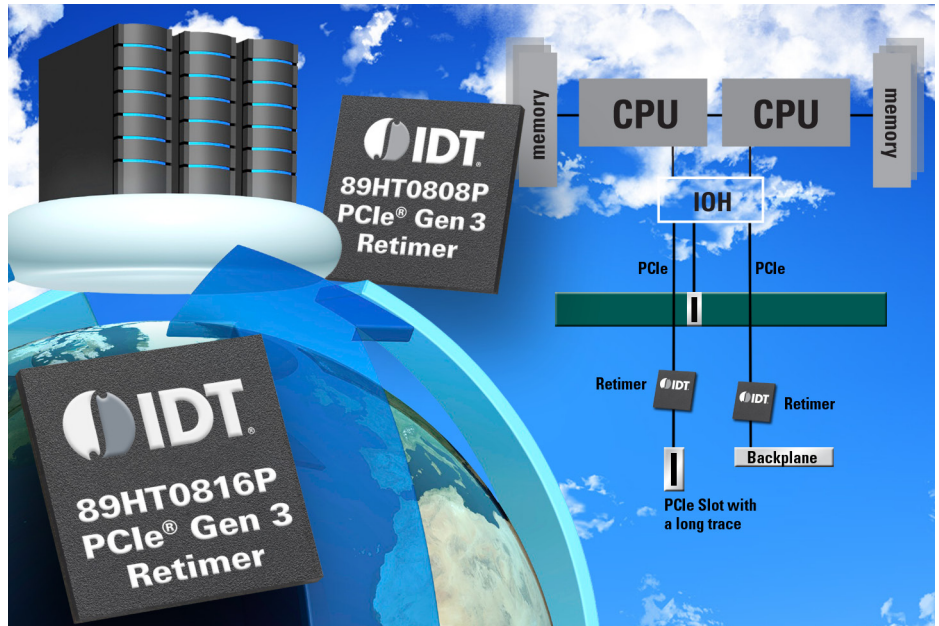
89HT0808P Signal Retimers

8 Channel Signal Retimers for 8.0Gbps, 5.0Gbps and 2.5Gbps PCIe®

POWER MANAGEMENT | ANALOG & RF | INTERFACE & CONNECTIVITY | CLOCKS & TIMING | MEMORY & LOGIC | TOUCH & USER INTERFACE | VIDEO & DISPLAY | AUDIO

FEATURES

- **High Performance Retimer**
 - Eliminates random input jitter
 - Eliminates deterministic ISI jitter
 - Compensates for PCB trace and cable attenuations
 - Performance and power tunable for each data rate
 - Wide swing, transmit driver offers up to 8dB of transmit deemphasis to meet the needs of the most challenging of backplanes
 - Multi-stage equalizer: CTLE and 5 tap DFE
 - Fast acquisition PLL for L0s exit
 - SERDES Rx eye generation (on-chip)
- **PCIe Standards and Compatibility**
 - PCI Express Base Specification 3.0 compliant
 - PCI Express Base Specification 2.1 compliant
- **Power Management**
 - Low power
 - Supports the following optional PCI Express features
 - L0s ASPM
 - L1 ASPM
- **Hot Plug Support**
- **SerDes Power Savings**
 - Supports low swing (half-swing) SerDes operation
 - SerDes associated with unused lanes are placed in a low power state automatically
- **Link Configurability**
 - Links can be configured with 1x4, 1x1, 2x1
 - Automatic per port link width negotiation (e.g., a x4 port can link train to x4, or x1)
 - Per-lane SerDes configuration
 - De-emphasis, receive equalization, drive strength
- **Clocking**
 - Uses standard 100 MHz PCIe reference clock
 - SSCLK (Spread Spectrum Clocking) supported with common clock configuration
 - Non-SSCLK supported with common and non-common clock configuration
- **I²C Interface**
 - Dedicated master interface
 - External EEPROM configuration loading
 - Dedicated slave interface
 - Configuration loading
 - Writing new or initial image into external EEPROM
 - Expose internal global CSR space to system controller
- **Reliability, Availability and Serviceability (RAS)**
 - Physical layer error checking and accounting
 - End-to-end data path parity protection
 - Checksum Serial EEPROM content protected
- **Test and Debug**
 - Per link/lane error diagnostic registers
 - All registers accessible from I²C, or JTAG port
 - SerDes test modes
 - Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG
 - Several loopback modes
- Packaged in a 9x9 mm, 100-pin BGA, 0.8 mm ball spacing



General Description

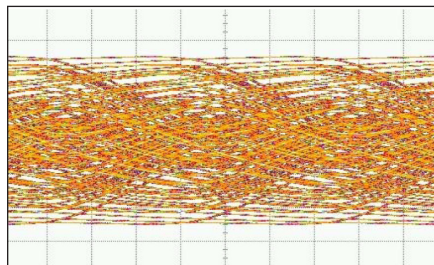
The 89HT0808P is a Signal Retimer/Conditioners used to improve signal integrity for enhancing system performance and reliability across long PCB traces or cables. It removes both random and deterministic jitter from the input signal eliminating inter-symbol interference, and resets the output jitter budget. It provides eight differential, 8Gbps PCIe Express® 3.0 channels, supporting up to 4 full lanes. It also fully supports PCIe Express 5Gbps and 2.5Gbps features. The T0808P is targeted to meet the high-performance needs of PCIe® Gen 3/2/1 applications.

Applications

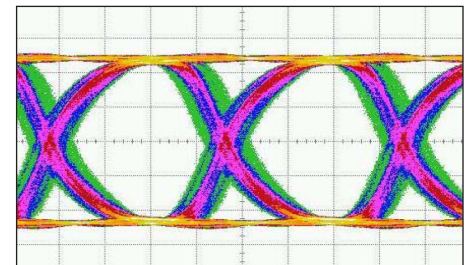
IDT's Retimer products fit into server, storage, and blade products, as well as Consumer Electronics and Communications applications.

Improving Signal Integrity with IDT Retimers

No Retimer



With IDT Retimer



Example Eye diagram FR4 and PRBS patterns

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties. IDT's products are not intended for use in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners. © Copyright 2010. All rights reserved.

PB_89HT0808P_REVA1110