



# IDT™ Programmable Clock Devices

## IDT Programmable Clock Devices

The IDT family of programmable clocks includes an advanced set of clock generation and distribution devices that support in-system programming and test. These devices can be configured or reconfigured at any point during the manufacturing process or end product's life cycle. This versatility, coupled with an advanced architecture and feature set, provides a compelling proposition to every segment of IDT customers. Designers benefit from these devices' high-resolution PLLs, broad feature set

and leading jitter performance. Manufacturers can utilize the in-system programming and test capabilities to reduce their costs and cycle times. Supply-chain managers enjoy a marked reduction in inventory complexity and cost as well as the potential to extend product life cycles through the non-volatile programming capability.

### Multi-PLL Clock Generators Consolidate Frequency Synthesis

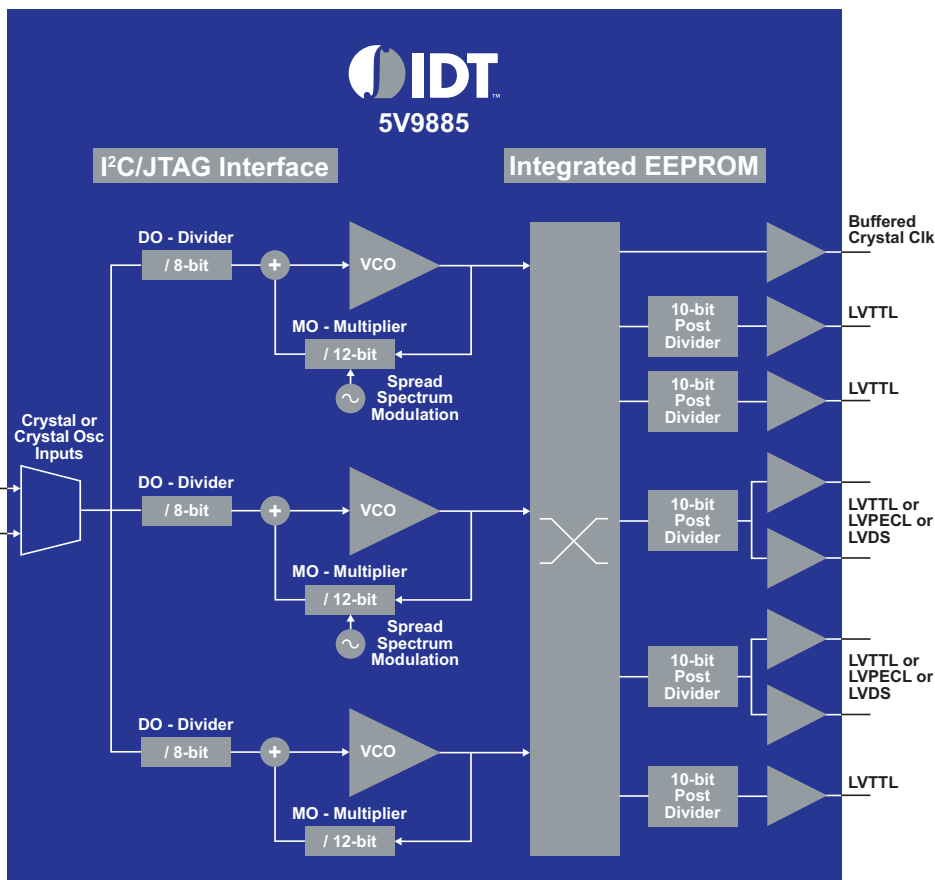
The IDT5V9885 programmable clock generator

### IDT creates preemptive semiconductor solutions that accelerate packet processing for advanced network services.

By anticipating the needs of equipment designers in the core, metro, access, enterprise, small office/home office (SOHO), data center and wireless segments of the network, IDT has created an industry-leading portfolio of semiconductor ICs. Our clock distribution and generation products enable the best performance in high-speed telecommunication, networking and storage area network equipment by offering leading-edge I/O standards and precise, reliable timing performance. We also offer network search engines (NSEs), flow-control management ICs (FCMs), multi-protocol switch fabric and traffic management chipsets, the Interprise™ family of integrated communications processors, FIFOs, multi-ports, and telecommunication ICs, as well as high-performance digital logic ICs and high-speed SRAM devices. Use IDT solutions to accelerate and enhance your network equipment designs.

is based on an innovative three-PLL architecture that includes ultra-high-resolution prescalers, multipliers and output dividers. With VCO ranges up to 1.1 GHz, nearly any combination of clock scaling ratios from a single input frequency is possible. The IDT5V9885 can replace multiple crystal oscillators and is ideal in any system that requires clock frequency translation or multiple clock domains. Leading-edge features such as programmable spread spectrum generation and glitchless input switching provide additional tools to the designers of next-generation clock networks.

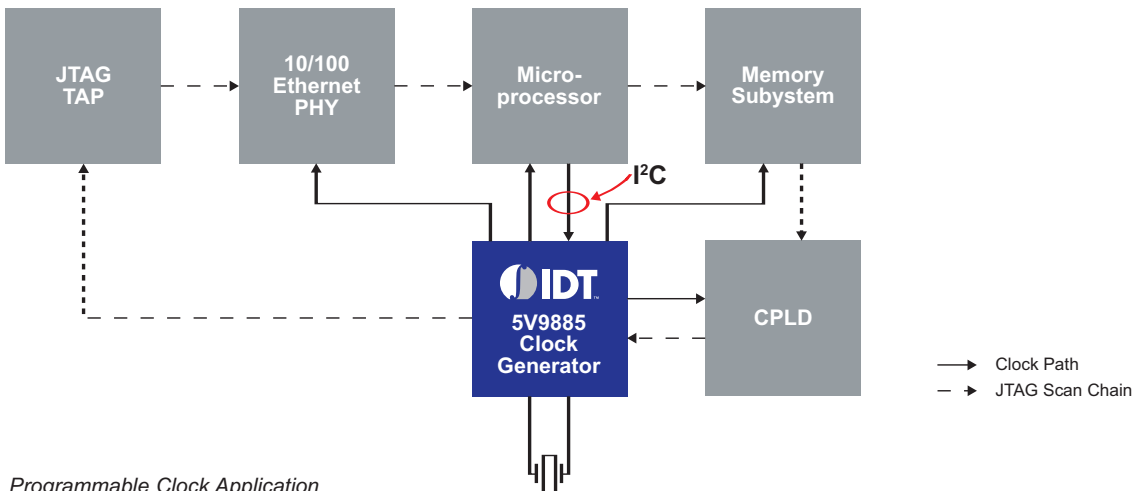
Development and evaluation kits for the entire family are available. Please contact your local IDT sales representative.



The 5V9885 integrates spread spectrum generation and 3 independent PLLs, each with very granular multipliers and dividers

# IDT™ Programmable Clock Devices

Features	Benefits
Complete family includes clock generation, programmable skew and zero delay buffer devices	"One-stop shop" for versatile clock network designs
"In system" programmable with integrated EEPROM	Device register settings can be saved, restored and/or reprogrammed in non-volatile memory. This allows: <ul style="list-style-type: none"> <li>- Reduced procurement costs and simplified logistics</li> <li>- Increased design portability and lifespan</li> <li>- Remote maintenance, modification and testing</li> </ul>
IEEE 1149.1 compliant JTAG boundary scan and programming via a single Test Access Port (TAP)	Simplifies system and board-level Design For Test (DFT) by allowing equipment to perform both boundary scan testing and programming Eliminates the need for test clock insertion via external equipment or dedicated boundary scan clock control
Three independent PLLs with high-resolution prescalers, multipliers and output dividers	Unmatched flexibility in clock scaling ratios to support nearly any combination of output frequencies from a single input frequency
Advanced I/O support: Input: Universal input supports any differential or single-ended logic type Output: 3.3V LVTTTL, LVPECL, LVDS	Provides I/O translation and enables applications that require various types of output logic
Supports output clocks up to 550 MHz	Versatile capability for a range of applications with maximum output frequency capability exceeding competing devices
High-performance PLL design with programmable loop filter minimizes jitter and skew	Meets demanding requirements of many communications, storage, consumer and industrial applications
Spread spectrum modulators with programmable spread characteristics including frequency, ratio and shape of the modulating waveform	Gives designers another tool to minimize EMI and pass stringent regulator requirements



Programmable Clock Application

01001001010000100001010100

## Programmable Clock Devices

Part Number	Input	Output	Number of Inputs	Number of Outputs	Input Frequency	Output Frequency	Multiply	Divide	Supply Voltage	Package
<b>Clock Generators</b>										
5V9885	3.3 V LVTTTL	3.3V LVPECL 3.3 V LVTTTL, LVDS	2 + 1 XTAL	8	1-400 MHz	.0049-550 MHz	12-bit	8-bit pre 10-bit post	3.3 V	TQFP 32 VFQFPN 28
<b>Zero Delay Buffers</b>										
5T9820	2.5 V/1.8 V LVTTTL 2.5 V/1.8 V HSTL 2.5 V/1.8 V eHSTL 2.5 V/1.8 V LVEPECL	2.5 V/1.8 V LVTTTL 2.5 V/1.8 V HSTL 2.5 V/1.8 V eHSTL	2	5 X 2, 1 X Diff	4.17-250 MHz	12.5-250 MHz	1-12	2, 4	2.5 V	VFQFPN 68
5T9821	2.5 V/1.8 V LVTTTL 2.5 V/1.8 V HSTL 2.5 V/1.8 V eHSTL 2.5 V/1.8 V LVEPECL	2.5 V/1.8 V LVTTTL 2.5 V/1.8 V HSTL 2.5 V/1.8 V eHSTL	2	6	4.17-250 MHz	12.5-250 MHz	1-12	2, 4	2.5 V	VFQFPN 68
<b>Programmable Skew Buffers</b>										
5T9890	2.5 V/1.8 V LVTTTL 2.5 V/1.8 V HSTL 2.5 V/1.8 V eHSTL 2.5 V/1.8 V LVEPECL	2.5 V/1.8 V LVTTTL 2.5 V/1.8 V HSTL 2.5 V/1.8 V eHSTL	2	6	4.17-250 MHz	12.5-250 MHz	1-12	2, 4	2.5 V	VFQFPN 68
5T9891	2.5 V/1.8 V LVTTTL 2.5 V/1.8 V eHSTL 2.5 V/1.8 V LVEPECL	2.5 V/1.8 V LVTTLL 2.5 V/1.8 V HSTL 2.5 V/1.8 V eHSTL	2	6	4.17-250 MHz	12.5-250 MHz	1-12	2, 4	2.5 V	VFQFPN 68

### Evaluation Boards

### Description

5V9885 EVB1	5V9885 Evaluation Board
98TDP – KT1	Programmable Clock Device Programmer
5V9885-NL-M1	5V9885NLGI Programming Module
5V9885-PF-M1	5V9885PFGI Programming Module
5T989x-982x-M1	5T989x-982x Programming Module

# IDT™ Programmable Clock Devices

## Arbor Clock Tree Design Service

Designing the optimum clock tree is an arduous and time-consuming task; therefore, IDT has created a service to do the design for you. The IDT Arbor Program Clock Tree Design Service eliminates the need for you to manage the clock tree design. The process begins with a designer and an IDT applications

engineer detailing the specifications; i.e., input frequencies, output frequencies, output signaling, output loads, jitter and skew. IDT will return a completed clock tree that meets design requirements and constraints, which may include a combination of IDT and IDT competitors' products. Because this is a

“design” service, IDT focuses on providing the designer with an overall solution, rather than selling its own products. For more information regarding this free service, visit <http://www.idt.com/?id=163>

### **CORPORATE HEADQUARTERS**

Integrated Device Technology, Inc.  
6024 Silver Creek Valley Road  
San Jose, CA 95138  
United States  
800 345 7015  
+408 284 8200 (outside U.S.)

### **ASIA PACIFIC AND JAPAN**

Integrated Device Technology  
Singapore (1997) Pte. Ltd.  
Reg. No. 199707558G  
435 Orchard Road  
#20-03 Wisma Atria  
Singapore 238877  
+65 6 887 5505

### **EUROPE**

Integrated Device Technology, Ltd.  
Prime House  
Barnett Wood Lane  
Leatherhead, Surrey  
United Kingdom KT22 7DE  
+44 1372 363339



**Accelerated Thinking<sup>SM</sup>**



Printed in USA 06-05/DSS/DL/HOP/3K

©2005 Integrated Device Technology, Inc. All rights reserved. Data subject to change without notice. IDT, and the IDT logo are trademarks of Integrated Device Technology, Inc. Accelerated Thinking is a service mark of Integrated Device Technology, Inc. All other brands, product names and marks are or may be trademarks or registered trademarks used to identify products or services of their respective owners.

FLYR-PCLOCK-00065